ARGUMENTS/REMARKS

STATUS OF CLAIMS

Claims 1 – 19 are pending after the foregoing amendment.

Claims 1 – 2 are withdrawn from consideration.

Claims 3 – 11 stand rejected.

Claims 12 – 19 are new.

Claim 4 has been amended to more clearly distinguish over the prior art. Support for the amendment is inherent in Paragraph [0025], for example.

Claim 6 has been amended, without prejudice or disclaimer, to conform the preamble to the preamble of claim 3, from which claim 6 depends.

Claim 8 has been amended, without prejudice or disclaimer, to correct an obvious error in wording.

New claims 12 -19 have been added. Support for claims 12 - 16 is found, for example, in Paragraph [0031] and Fig. 1. Support for claim 17 is found, for example, in Paragraph [0033] and Fig. 1. Support for claims 18 and 19 is found, for example, in Paragraph [0031] and Fig. 1b.

Restriction of claims 1-11

The Examiner has made final the requirement of restriction to Group I (claims 3 – 11) or Group II (claims 1 – 2). The applicant confirms the provisional election of the invention of Group I (Claims 3 – 11).

Rejection of claims 3-11 as anticipated by U.S. Patent No. 6,853,104 (Taylor, et al.)

Claims 3 -11 stand rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,853,014 (Taylor, et al.). The rejection is respectfully traversed, on the grounds that Taylor does not teach all of the limitations of the rejected claims.

As to claims 3 and 10, the Examiner states, on page 3 of the Office Action, that Taylor discloses an optoelectronic circuit with a first block comprising an enhancement mode PHEMT transistor on a substrate; a second block comprising a depletion mode PHEMT transistor on the substrate, the second block operatively connected to the first block; a third block comprising a power PHEMT transistor on the substrate, the third block operatively connected to at least one of the first block and the second block. The Examiner refers generally to column 29, line 1 to column 39, line 58, and Figs. 4A through 5F.

"'A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.' *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987)." MPEP 2131.

As to claim 3, the rejection is respectfully traversed on the grounds that Taylor neither teaches nor suggests at least the following limitations of claim 3:

"an enhancement mode pHEMT transistor on a substrate,"

"a depletion mode pHEMT transistor on the substrate," and

"a power pHEMT transistor on the substrate."

By way of background, a pHEMT, or pseudomorphic high electron mobility transistor, is a type of field effect transistor (FET), and more specifically a type of high electron mobility transistor (HEMT). In a HEMT there is a doped donor/undoped spacer layer of one material and an undoped channel layer of a different material. A heterojunction is formed between the doped donor/undoped spacer layer and the undoped channel layer. The doped donor layer has a wider bandgap than the undoped channel layer. Due to the conduction band discontinuity at the heterojunction, electrons are injected from the doped donor/undoped spacer layer into the undoped channel layer. Thus, electrons from the relatively large bandgap donor layer are transferred into the relatively narrow bandgap channel layer where they are confined to move only in a plane parallel to the heterojunction. In a pHEMT transistor, one or more of the layers incorporated into the device has a lattice constant which differs slightly from the lattice constants of other materials of the device. An enhancement-mode pHEMT transistor is a pHEMT transistor that blocks the flow of current when no gate-source voltage is applied (also called a normally-off transistor). A depletion-mode pHEMT transistor is a pHEMT transistor that allows current to flow when no gate-source voltage is applied (also called a normally-on transistor). Typically, the thickness of the active region upon which the gate contact is formed is different for depletion-mode pHEMT transistors and enhancement-mode pHEMT transistors, with this thickness being smaller for the enhancement-mode pHEMT transistor than it is for the depletion-mode pHEMT transistor. The voltage threshold between the two states of these transitions is known as the pinch-off voltage. The pinch-off voltage of a given device is dependent on the thickness of the active region on which the gate contact is formed. A power pHEMT is a depletion mode pHEMT characterized by higher drain operating voltage than a

conventional depletion mode pHEMT. Conventional depletion-mode pHEMT transistors customarily have a single recess structure. A power pHEMT transistor, by contrast, ordinarily features a double recess structure.

Thus, in order for Taylor to meet all of the limitations of claim 3, Taylor would need to teach, on the same substrate, an enhancement mode pHEMT transistor, and two types of depletion mode pHEMT transistors, characterized at least by differing drain operating voltages.

The structures of Taylor are not pHEMT transistors at all. Taylor makes this clear by characterizing its structures as: "novel device structures utilizing modulation-doped quantum well heterojunctions that do not suffer from the problems associated with the prior art PHEMT devices." (col. 13, lines 52 – 55). The device of Fig. 2A of Taylor is characterized as a heterojunction thyristor device (col. 13, lines 66-67). The layer structure of Fig. 2A appears to be the same as that of Figs. 4C and 4D (other than the absence of a top diffraction grating and DBR mirror), and Figs. 5C, 5D, which were pointed out in the Office Action as teaching the limitations of claims 3 and 10. Taylor further states that its heterojunction thyristor devices can be configured to operate as a field effect transistor, bipolar transistor, and in a passive waveguide (col. 14, lines 1-3). Thus, Taylor teaches a new structure, a heterojunction thyristor, which Taylor characterizes as overcoming disadvantages of pHEMT transistors. Taylor even teaches that a heterojunction thyristor is capable of operating as a field effect transistor, which is the class of transistors to which pHEMT transistors belong.

Moreover, the various structures taught by Taylor are not characterized as enhancement-mode or depletion-mode transistors. Thus, Taylor has no literal teaching

of both enhancement-mode and depletion-mode pHEMTs. Taylor does teach that its heterojunction thyristor devices may include HFET devices, having modulation doped quantum wells, which may be formed from strained heterojunction materials (col. 14, lines 20 – 50); however, there is no indication of structural differences, such as differing thicknesses of the active region over the gate contact, or of operational differences, such as differing pinch-off voltages and differing drain operating voltages, which would indicate that both enhancement-mode and depletion-mode pHEMT's, and both conventional depletion-mode and power pHEMT's, are included on the same substrate in Taylor.

Taylor fails to teach or suggest a power pHEMT, or the double recess structure ordinarily employed for a power pHEMT. Indeed, Taylor has no reference whatever to depletion mode pHEMT's having differing drain operating voltages. As there is no reference to power pHEMT's in Taylor, there is no suggestion that a power pHEMT on the same substrate as an enhancement mode pHEMT and a depletion mode pHEMT would be desirable.

The operation of the devices shown in the Figs. 4C, 4D, 5C and 5D, does not even appear to be that of a pHEMT. Indeed, these devices are characterized as thyristors, not as transistors. By way of example, the operation of the device of Fig. 4C is explained as follows at col. 31, lines 18-47.

> In FIG. 4C, a first p-channel injector terminal 222 (the electrical input terminal) and a second p-channel injector terminal 224 (the electrical output terminal) are operably coupled to opposite ends of the p-type QW channel(s) of structure 20. An electrical sampling clock pulse in the form of a downward running electrical pulse is supplied to the n-channel injector terminal(s) 226 of the device. In addition, a bias current source is coupled to the n-channel injector terminal(s) 226 and draws charge from the n-type

> QW channel(s) to the positive supply voltage potential V_D. The anode terminal 228 is forward biased (e.g. biased positively) with respect to the cathode terminal 230. The length and width of the device are sized such that it switches from a non-conducting/OFF state to a conducting/ON state when the electrical energy injected into the n-type QW channel(s) of structure 24 by the electrical sampling clock pulse produces a channel current that exceeds the bias current I_{BIAS} such that charge in the n-type QW channel(s) of structure 24 builds to a level that is greater than the critical switching charge Q_{CR}. When the electrical sampling clock pulse terminates, the bias current I_{BIAS} reduces the charge in the n-type QW channel(s) to a level below the holding charge Q_H, thereby causing the device to switch from the conducting/ON state to the non-conducting/OFF state. Note that the device does not switch from the non-conducting/OFF state to the conducting/ON state in the event that the electrical sampling clock pulse is not present. This occurs because there is no injection of electrical energy into the QW channel(s) of the device to produce the critical switching charge Q_{CR}.

Thus, rather than providing a gate that controls flow of current in the quantum well, as in a pHEMT, the charge in the quantum well controls the operation of the device of Taylor.

Furthermore, Taylor fails to teach or suggest a first block having at least one enhancement-mode pHEMT, a second block having at least one depletion-mode pHEMT, and a third block having at least one power pHEMT, each of the pHEMT's being on the same substrate, and being interconnected.

For at least the foregoing reasons, claim 3 is allowable.

Claim 10 includes all of the limitations of claim 3, and is allowable for the reasons that claim 3 is allowable.

Claim 4 has been amended to recite that the analog input and the digital output are both for electrical signals. It is clear from Paragraph [0025] that the inputs, outputs and devices described therein include electrical signal devices. Taylor, by contrast, teaches photonic digital-to-analog converters that convert digital optical signals to analog electrical signals (e.g., col. 10, lines 8-15). Moreover, Taylor's devices are specifically designed to provide optoelectronic interfaces, and thus do not provide a suggestion of electrical signal to electrical signal conversion.

For at least the foregoing reasons, as well as the reasons set forth above in connection with claim 3, claim 4 is allowable.

Claim 5 depends from claim 3, and adds the further limitation that the integrated circuit is a microwave and millimeter wave integrated circuit (MMIC). The Office Action indicates, on page 4, that Taylor teaches the limitations of claim 5 at col. 12, lines 42-59. This rejection is respectfully traversed. Taylor merely discusses, in this portion of col. 12, background information. Taylor nowhere teaches or suggests the use of the structures taught therein in microwave and millimeter wave integrated circuits. For at least this reasons, as well as the reasons set forth above in connection with claim 3, claim 5 is allowable.

Claim 6 depends from claim 3, and adds the further limitation that the integrated circuit is capable of operating at a frequency within the range of from very low frequency up to and including X-band frequencies. In order for this limitation to be taught in the prior art, a reference must teach a circuit capable of operating at this entire frequency

range; a circuit capable of operating at only a portion of this range does not teach the limitations of claim 6. The Office Action cites col. 12, lines 42-59 of Taylor, and col. 20, lines 42-50 of Taylor, as teaching the limitations of claim 6. As noted above in connection with claim 5, col. 12 of Taylor merely provides background information, and does not indicate an application of the structures taught in Taylor. The cited portion of col. 20 of Taylor discusses materials, and not ranges of operating frequencies. Taylor nowhere suggests circuits using its thyristor structures that operate at the entire range required by claim 6. For at least this reason, as well as the reasons set forth above in connection with claim 3, claim 6 is allowable.

Claim 7 is an independent claim reciting an analog to digital converter, having an enhancement mode pHEMT device, a depletion mode pHEMT device, and a power pHEMT device on a single substrate. For the reasons discussed above in connection with claim 3, Taylor does not teach or suggest these three types of devices at all, nor on a single substrate. For at least this reason, claim 7 is allowable.

Claims 8 and 9 depend from claim 7, and are allowable for the reasons that claim 7 is allowable.

Claim 11 depends from claim 10, and is allowable for the reasons that claim 10 is allowable.

New claims 12 – 19 depend directly or indirectly from claim 3, and are allowable over the prior art of record at least for the reasons set forth above in connection with claim 3.

CONCLUSION

Wherefore, Applicant believes he has addressed all outstanding matters, and respectfully requests that claims 3 – 19 be allowed.

Should there be any questions or outstanding matters, the Examiner is cordially invited and requested to contact Applicant's undersigned attorney at his number listed below.

Respectfully submitted,

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Attachments: 11 sheets of drawings